NOνA Power Distribution Box Testing

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Version 1.0

The NOνA Power Distribution Box distributes power to the front end boards, thermoelectric cooler, and avalanche photodiodes. The testing of a Power Distribution Box (PDB) is described in the following document. This document provides the details of this testing and serves as a User's Manual. These tests were used for the Near Detector PDBs made in the summer of 2010.

I. Introduction

Figures 1-4 show the major components of the NOνA Power Distribution Box (PDB) and introduce the terminology used in this document.

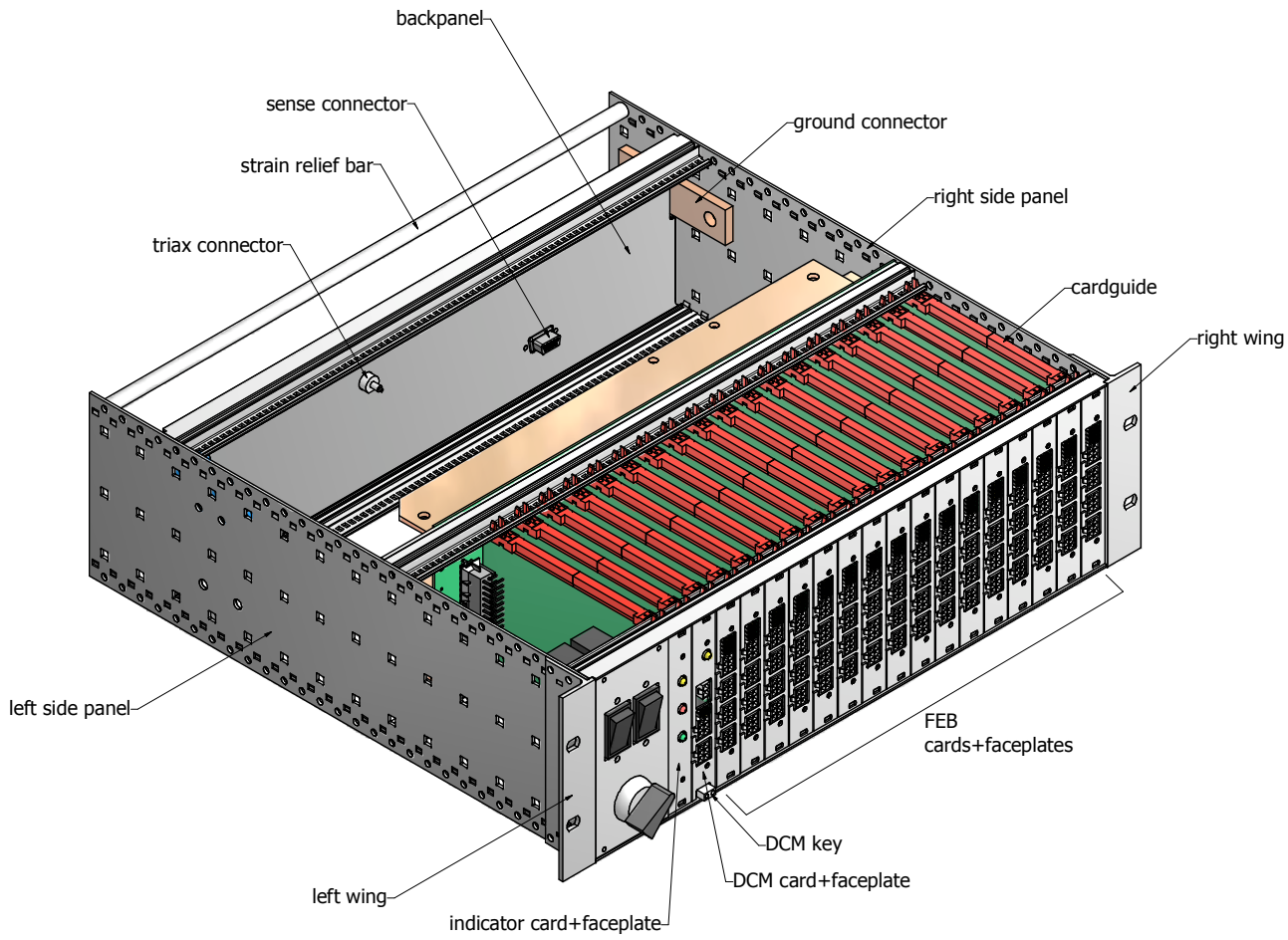


Figure 1. NOνA Power Distribution Box.

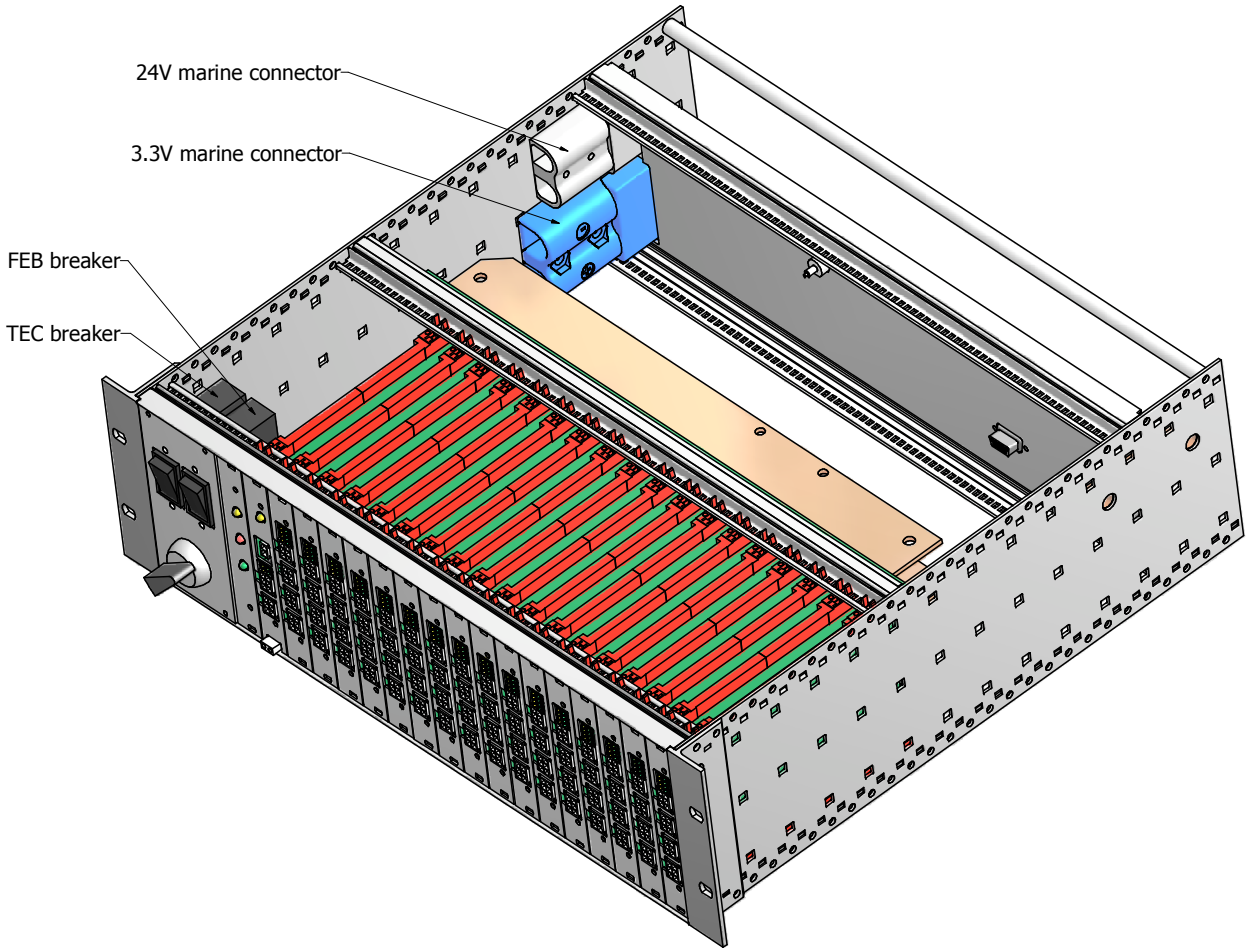


Figure 2. NOνA Power Distribution Box.

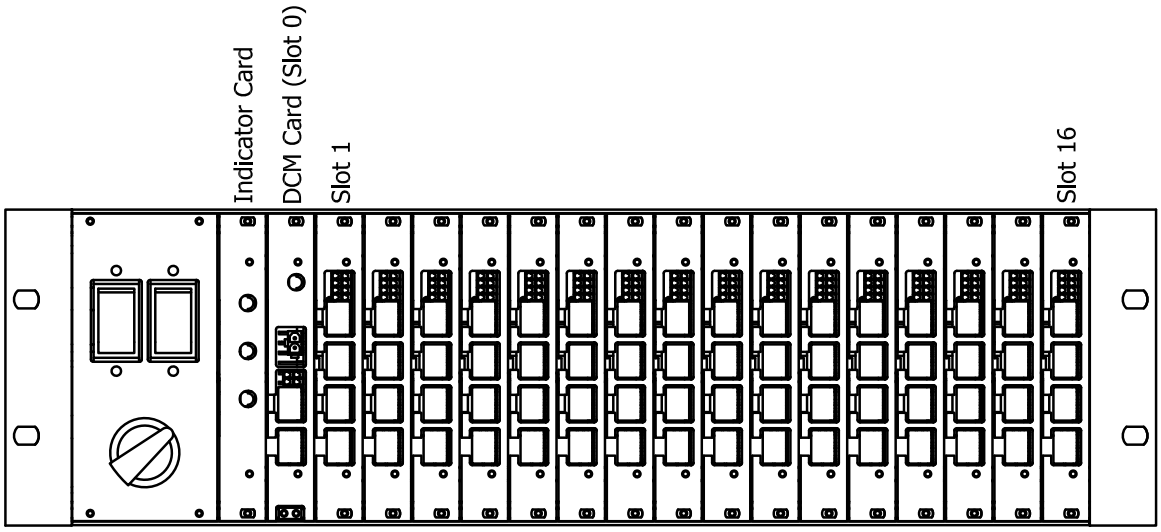


Figure 3. Numbering of the "slots".

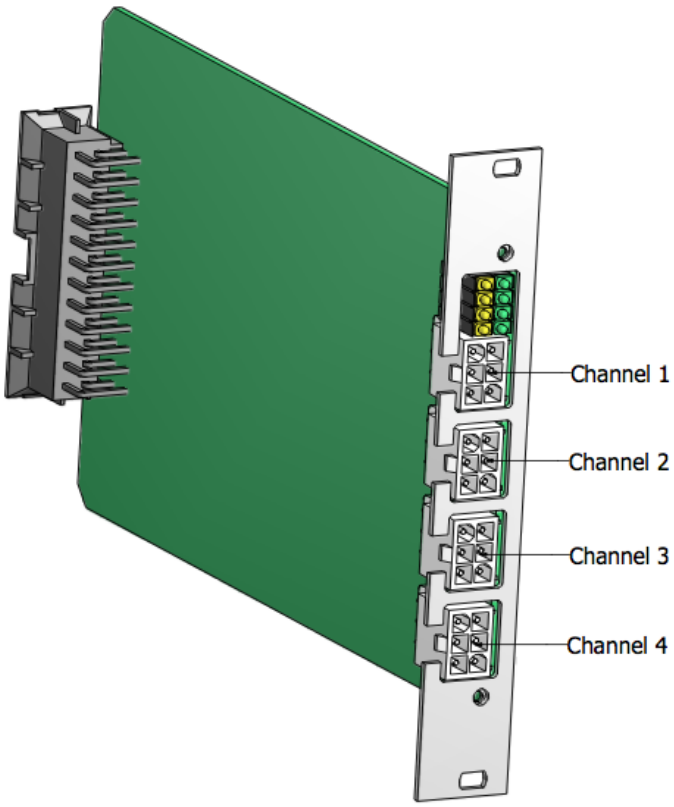


Figure 4. Numbering of the channels of an FEB card.

The NOνA Power Distribution Box (PDB) is used to distribute power from power supplies to the front end boards, thermoelectric coolers, and avalanche photodiodes on the NOνA detectors. The PDBs are also used to power the Data Concentrator Modules (DCMs). Approximately 10 PDBs are required for the Near Detector and 180 for the Far Detector. The PDBs are mounted on the top and side of the detectors. The FEB cards in the PDBs (shown in Figure 4) have four channels and each channel supplies 3 voltages. One PDB can hold up to 16 FEB cards. Each channel of an FEB card gets connected to an electronics box on the detector and powers the front end board (FEB), thermoelectric cooler (TEC), and avalanche photodiode (APD) in that box. There is also one DCM card per PDB which has two channels like those on the FEB cards and one channel to power a DCM. Table 1 shows the nominal power requirements for NOνA electronics.

Module	Voltage	Current
FEB	3.3 V	1.0 A
TEC	24 V	0.15 A
APD	350-450 V	40 μA
DCM	24 V	2.0 A

Table 1. Nominal power requirements.

At UVa we have developed a system to test the power output capabilities of the PDBs under load. The testing is carried out using LabVIEW running on a National Instruments PXI crate. Three power supplies provide three different voltages to the PDBs and three programmable electronic loads are used to put the DCM and FEB cards under load. Testing is split into two parts: one LabVIEW program is used to test the empty PDBs and a second LabVIEW program is used to test the cards that get put into the PDBs. Testing a PDB involves verifying that all the components are connected properly and that all the channels of the backplane function properly. A prototype PDB is used to test the cards, which involves measuring the current and voltage outputs of the cards under load. For each test the three power supplies are configured to run at 445V, 30V, and 6V.

For each test, with the system under load, current and voltage measurements are taken on all the power supplies and all the electronic loads through LabVIEW. LabVIEW opens an Excel spreadsheet and begins populating it with this data. Once all the data has been collected, LabVIEW checks the data in the Excel spreadsheet against a range of acceptable values. Any values that fall outside of the acceptable range are recorded on the spreadsheet. See Section III for step-by-step instructions on running the tests. For information about the LabVIEW test programs, see Section IV. See Section V for information on data analysis.

II. Test Apparatus

Figures 5 and 6 show the test setup. There are three power supplies: The Spellman/Bertan [1] 205-B-03R provides high voltage (445V for these tests), the Agilent [2] N5761A provides 6V, and the Agilent N5765A provides 30V. There are two PDBs mounted on the relay rack. The upper PDB is the empty PDB being tested along with its installed backplane. The lower PDB is a prototype PDB which is used to test Indicator, DCM, and FEB cards. After testing the upper PDB, it gets switched out with the next PDB to be tested. The lower PDB is never removed, providing a consistent testing platform for all of the cards. A fan is mounted between the two PDBs to cool the upper PDB during a backplane test.

Figure 5. Testing station.

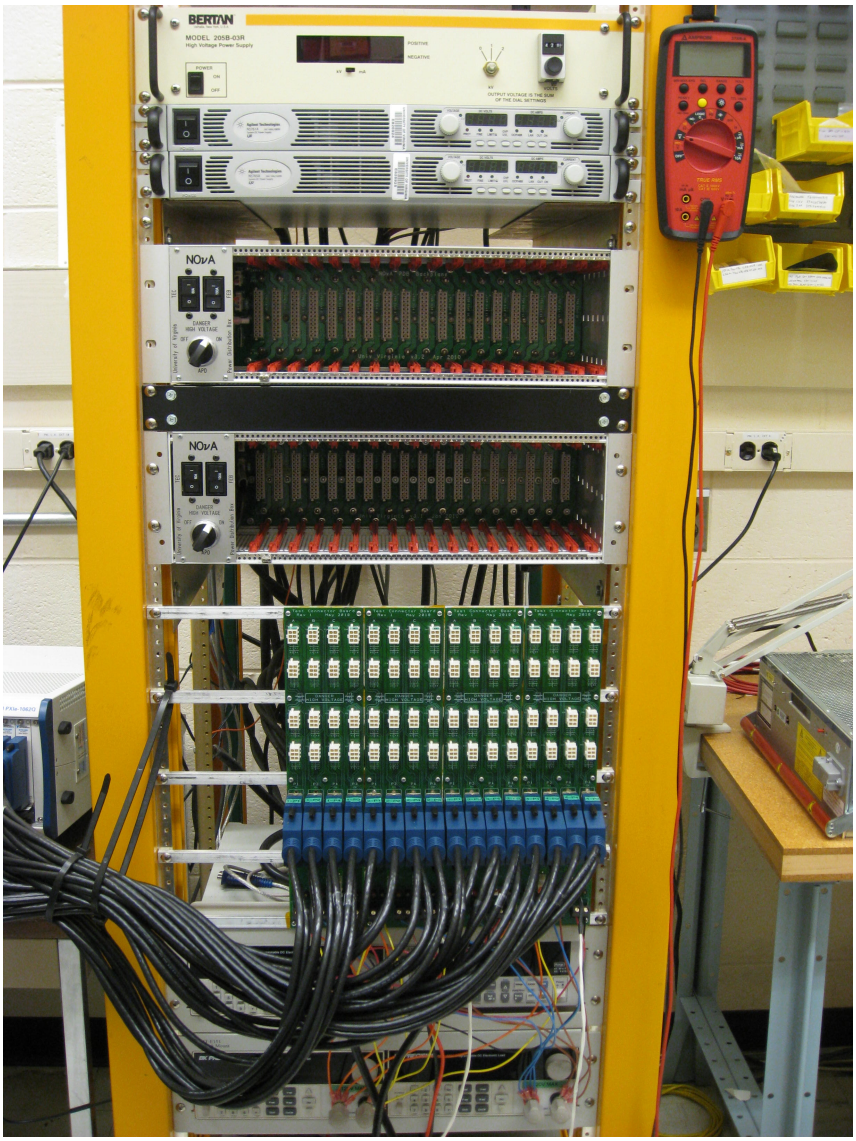


Figure 6. Test rack.

The output of each card in a PDB is routed to one of the Test Connector Boards. The Test Connector Boards were designed and manufactured by Stephen Goadhouse, a UVa electrical engineer. Figure 7 shows the cabling setup for testing the cards. The FEB cards are connected using six conductor 18AWG cables terminated at both ends with TYCO MINI MATE-N-LOK 6 pin headers (this is the standard FEB cable) [3]. The 24V DCM card channel is connected to the Test Connector Boards with 18AWG cables terminated at one end with a TYCO MINI MATE-N-LOK 2 pin header, while the other end is split and both ends are terminated with the same header. The two FEB channels on the DCM card use specially made cables because of the way the DCM FEB channels had to be broken up to accommodate the Test Connector Board.

When testing the PDBs, load boards containing resistors are used in place of FEB and DCM cards. The load boards are plugged into the backplane of a PDB to provide a load. The load boards use the same fab as the FEB cards and are connected to the Test Connector Boards just as the FEB cards are when testing the cards in the prototype PDB. See Figure 9 for a cabling diagram. The DCM load board uses the same fab as the FEB load board but with different resistors: the resistors for the 3.3V voltage on the DCM channels are removed and the resistors for the 24V voltage are different. Also, channels 1 & 4 are FEB channels and channels 3 & 4 are DCM channels. The loads boards are numbered and should be placed in the corresponding slot (Figure 3). This is important because resistance measurements have been recorded for each load board and are used in calculations.

During testing of the cards the system is put under load with programable BK Precision e-loads connected to the Test Connector Boards, with the loads being switched on and off by relays controlled through LabVIEW. Current and voltage data from the e-loads is recorded. When testing the PDBs no load is applied through the Test Connector Boards (since load boards are being used in the PDB) and the e-loads are used as measurement devices. Three load modules are used. The BK Precision 8502 is the HV load, the 8500 on the left is the 3.3V load, and the 8500 on the right is the 24V load. The cables connecting the e-loads are 18AWG with one end terminated with a ring terminal while the other end connects to the Test Connector Board at a screw terminal.

The Agilent power supplies and all three e-loads communicate with a National Instruments PXIe-1062Q crate via a USB hub (Figure 11). Both Agilent supplies have a direct USB output routed to the hub. Each e-load connects with an IT-E131 RS232 Communication Cable (RS232 $\Longleftrightarrow$ Isolation $\Longleftrightarrow$ TTL) linked with a Serial RS232 to USB Cable (using the FTDI chipset). The RS232 to USB cable we used is Digi-Key Part # 768-1013-ND. To control the loading we used NI PXI-2569 100 SPST Relay Modules with NI 192004C-01 Type SH200LFH-4XDB50F-C 1 meter cables. These relays are rated to 60V and can switch up to 1A. On the back of the HV supply are two switches, S101 and S102, which have been set to Remote and Analog, respectively.

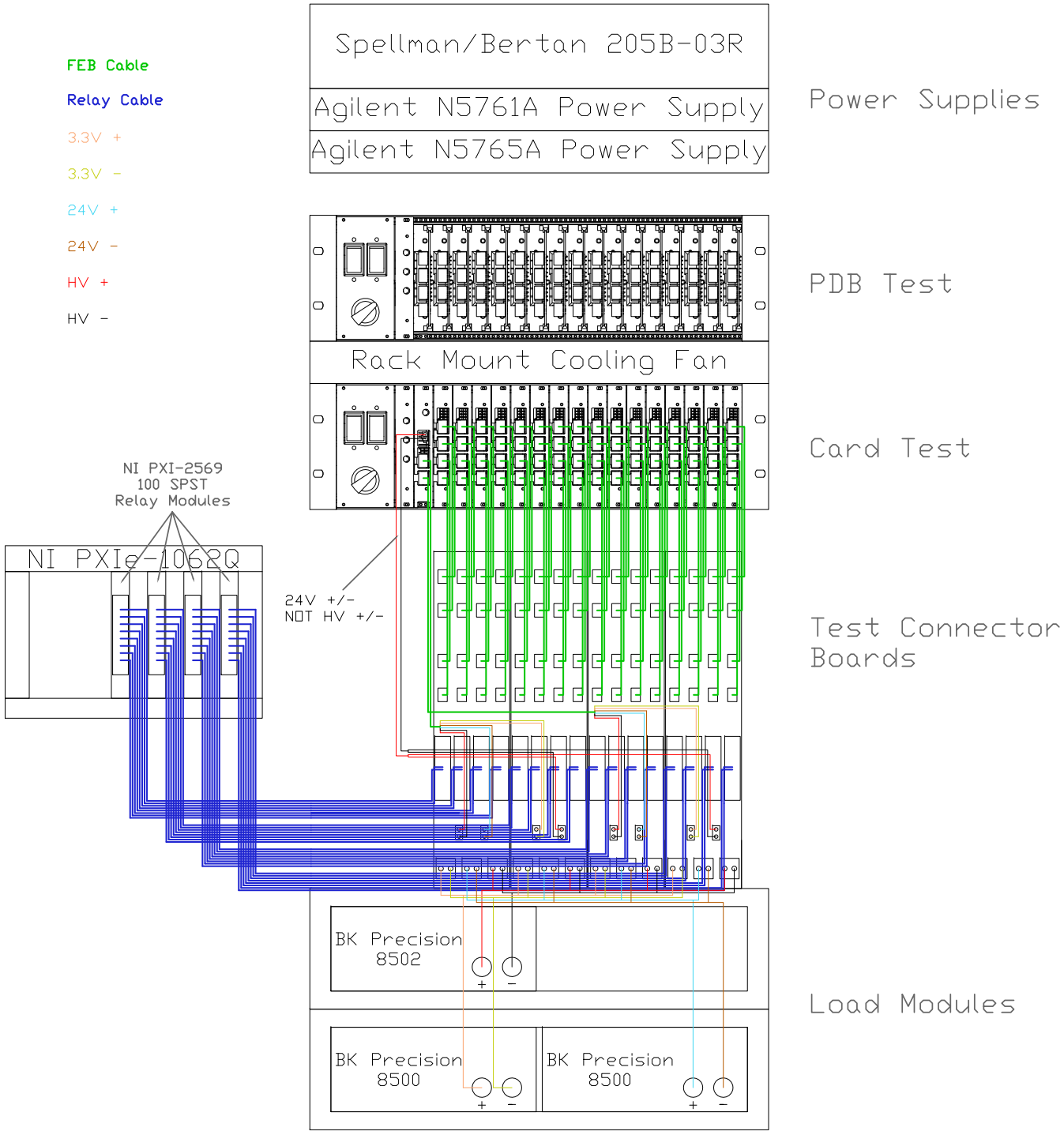


Figure 7. The PDB test rack showing the cable routing.

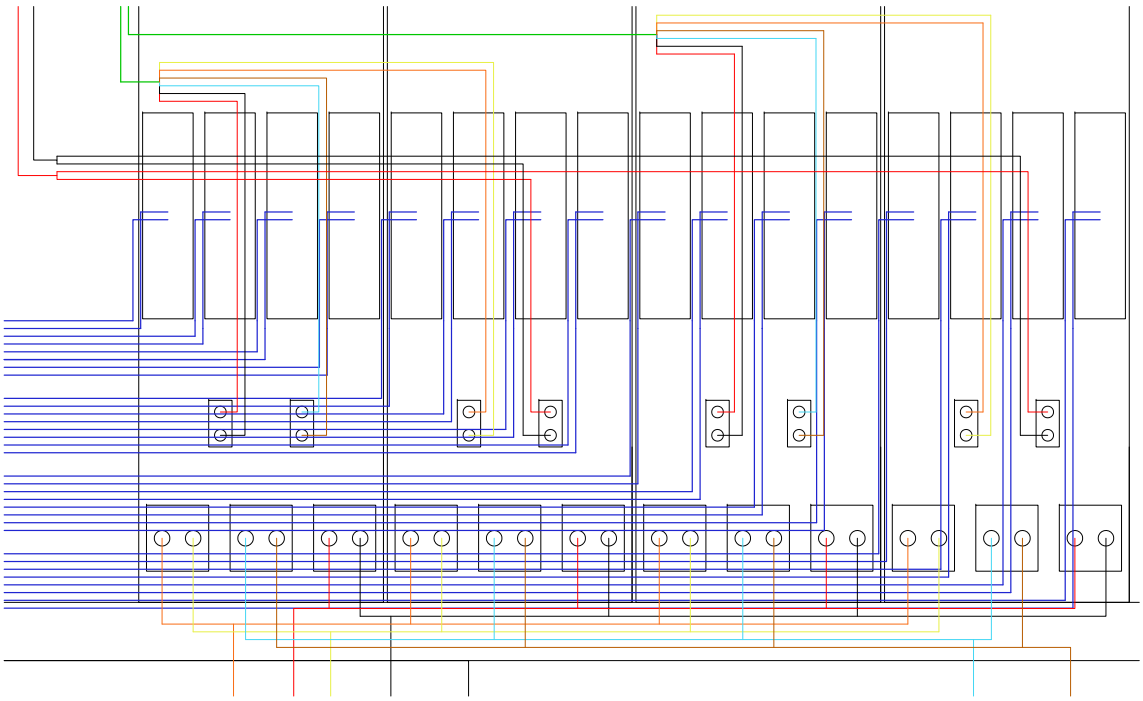


Figure 8. Close up of the PDB wiring showing the Test Connector Boards.

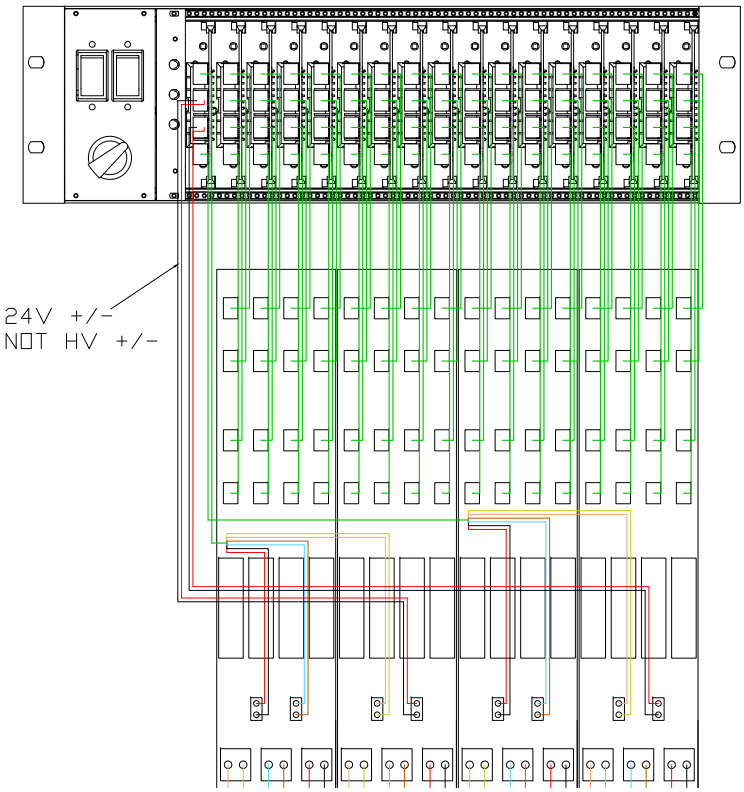


Figure 9. Cabling for load boards in upper PDB (prototype PDB and relays not shown).

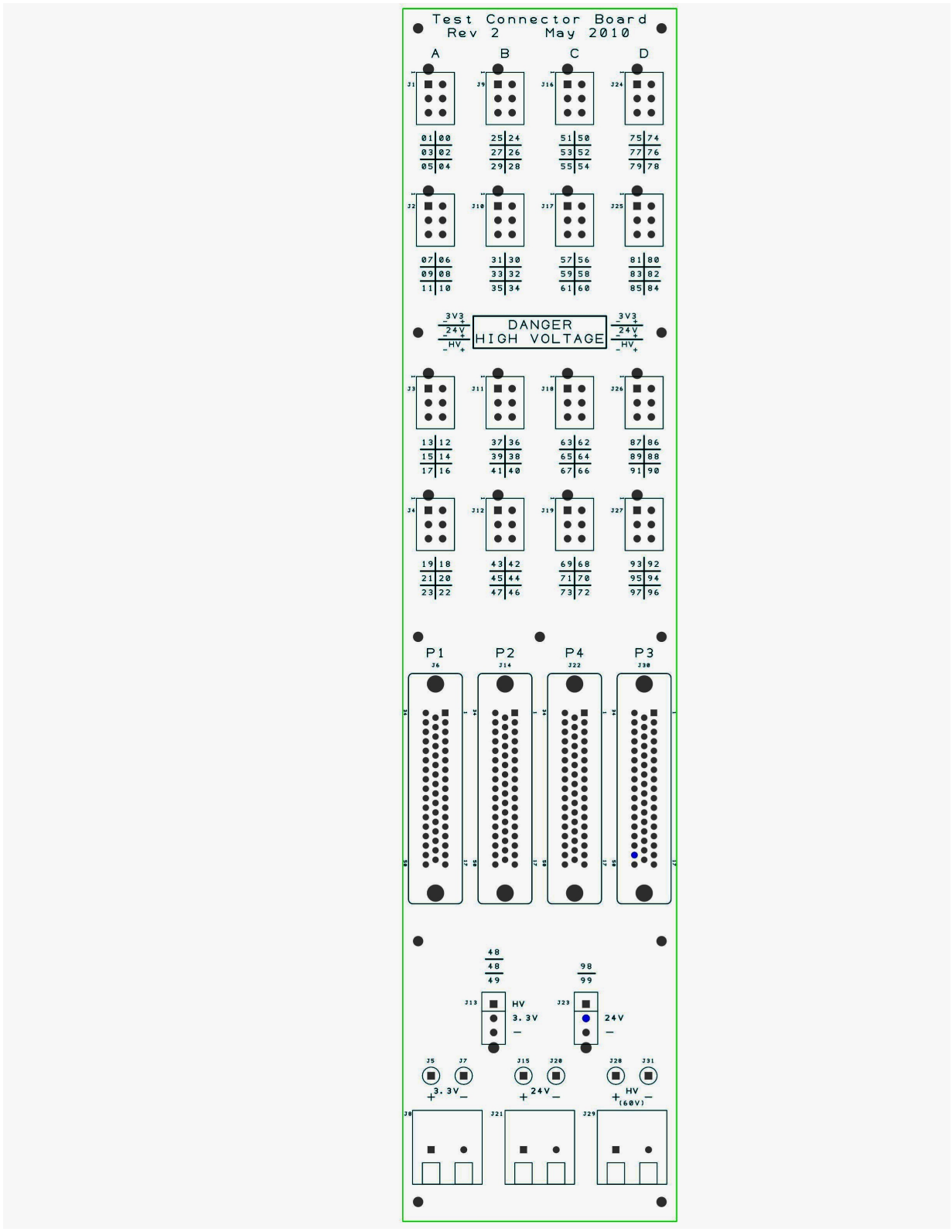


Figure 10. Test Connector Board header layout.

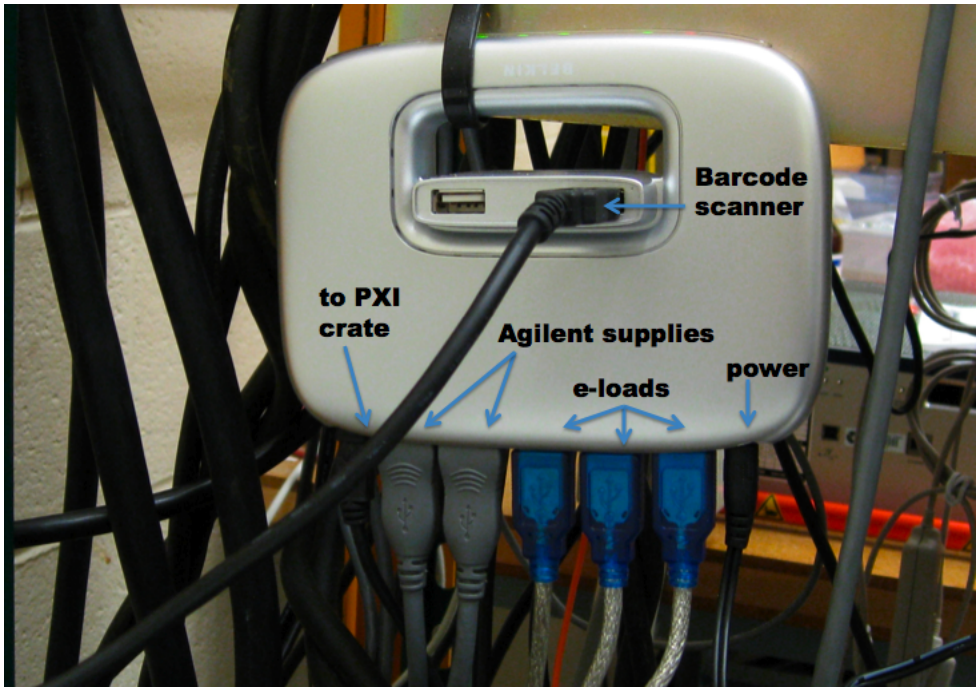


Figure 11. USB hub connecting the e-loads and the power supplies to the PXI crate.

The following parameters in the BK Precision CONFIG menu have been changed from the default:

RANGE SELECT: ON

ADC UPDATE RATE: HIGH

BAUDRATE SET: 38400

Note: After setting RANGE SELECT to ON, exit the CONFIG menu and press Shift + $\bigtriangledown$ and Shift + $\bigtriangleup$ to allow for the best current and voltage resolutions. This should only have to be done once during initial setup.

The PXI crate contains an NI PXI-7851R RIO card (Reconfigurable I/O) that is controlled through LabVIEW FPGA modules. The RIO card is used during the Current Limit Test to collect data. Connected to Connector 0 of this card is an SCB-68 Terminal Block used to connect the analog output of the HV supply to the RIO. The table below describes the testing configuration. The DB9 connector is the control and monitoring interface for the HV supply. The FPGA I/O column in Table 2 contains the resource name used by LabVIEW.

DB9 Pin	SCB Terminal	FPGA I/O	HV Power Supply Function
1	68	AI0	Buffered output voltage monitor, 0 to +5VDC via 10KΩ. The analog signal has a linear scale with 0VDC meaning 0V HV output and +5VDC meaning 3kV HV output (max output voltage).
2	No Connection	N/A	No Connection
3	No Connection	N/A	TTL level compatible logic input. Input logic zero disables high voltage generation. Open circuit or input logic one enables high voltage generation.
4	No Connection	N/A	Precision +5VDC reference output, referenced to analog ground.
5	66	AI1	Buffered output current monitor, 0 to +5VDC via 10KΩ. The analog signal has a linear scale with 0VDC meaning 0mA HV output and +5VDC meaning 10mA HV output (max output current).
6	55	AO0	Remote analog programming input, 0 to +5VDC. Input of 0V programs the HV output to be 0V and input of 5VDC programs the HV output for maximum voltage, which is 3kVDC. Analog input is also linear so that 0.742V = 445VDC.
7	56	None	Analog ground
8	2	None	Digital ground
9	47	DIO15	NPN open collector with respect to digital ground, indicating output high voltage polarity. NPN saturation denotes positive polarity (logic 0), NPN cut-off denotes negative polarity (logic 1). This value is not recorded.

Table 2. SCB-68 terminal block configuration.

The function of DB9 pin 3 given in Table 2 is the documented function in the HV supply user manual but the actual pin is an unknown 15V signal and so it is not being used due to this discrepancy. Terminals 21 and 56 are jumpered within the SCB housing. Terminals 1 and 47 have a 4.3kΩ resistor across them, with terminal 1 at 5V. This resistor is also connected within the SCB housing. The cable from the DB9 to the SCB-68 is a shielded 6C cable, the same as used for the PDB sense connector. The cable shielding is soldered to a

shield lug within the SCB-68 housing. There are five switches inside the SCB-68 and they are in the general purpose configuration as shown in Figure 12.

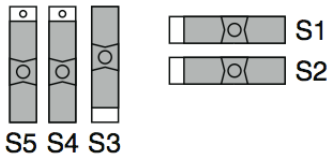


Figure 12. General purpose switch configuration for SCB-68 terminal block.

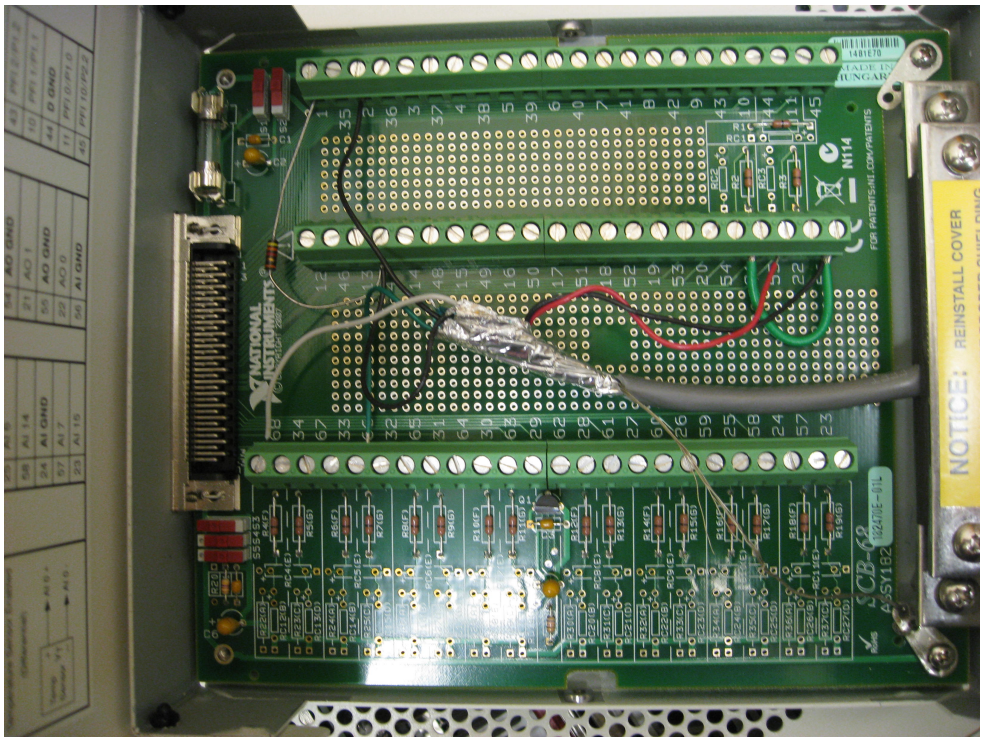


Figure 13. View of the SCB-68 terminal block with the cover removed.

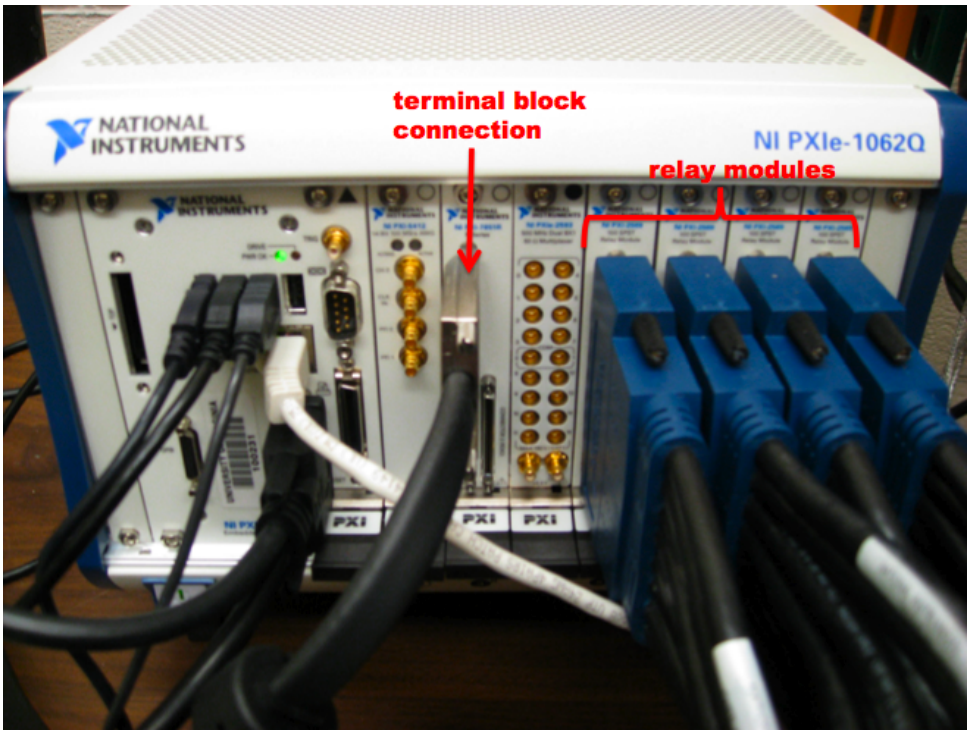


Figure 14. National Instruments PXI crate.

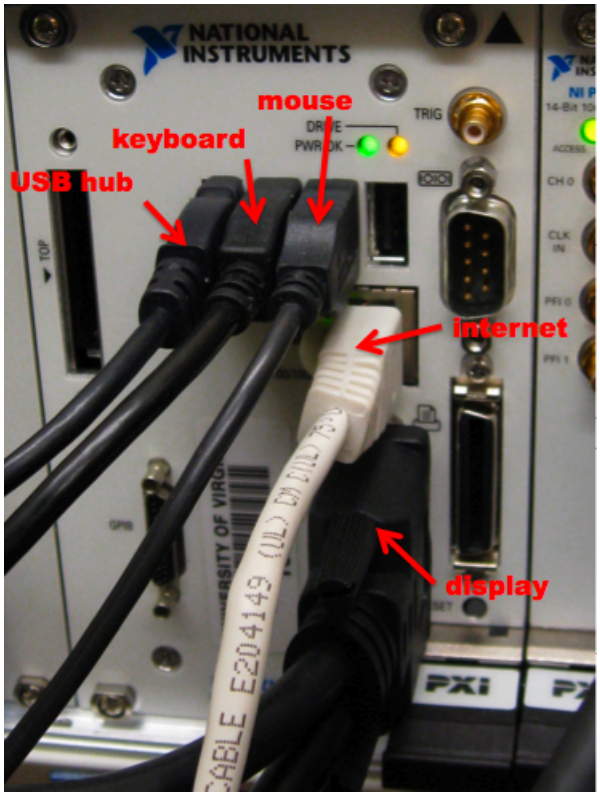


Figure 15. Closer view of panel on PXI crate showing USB connections.

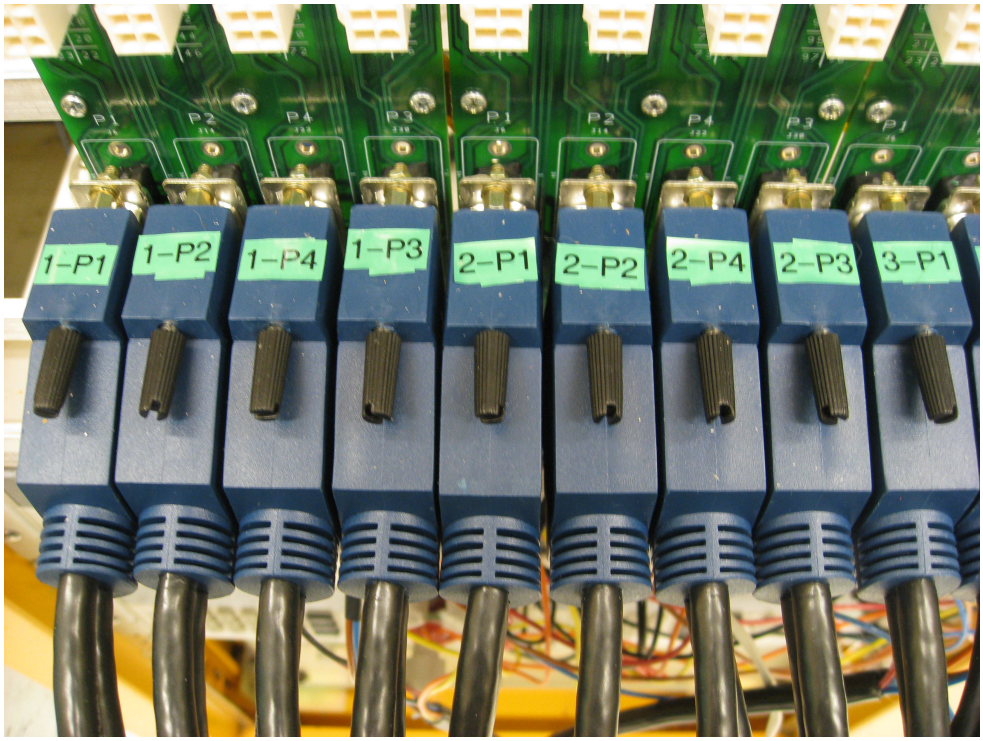


Figure 16. Numbering of the relay connectors on the Test Connector Boards. From left to right on each board it goes 1-2-4-3.

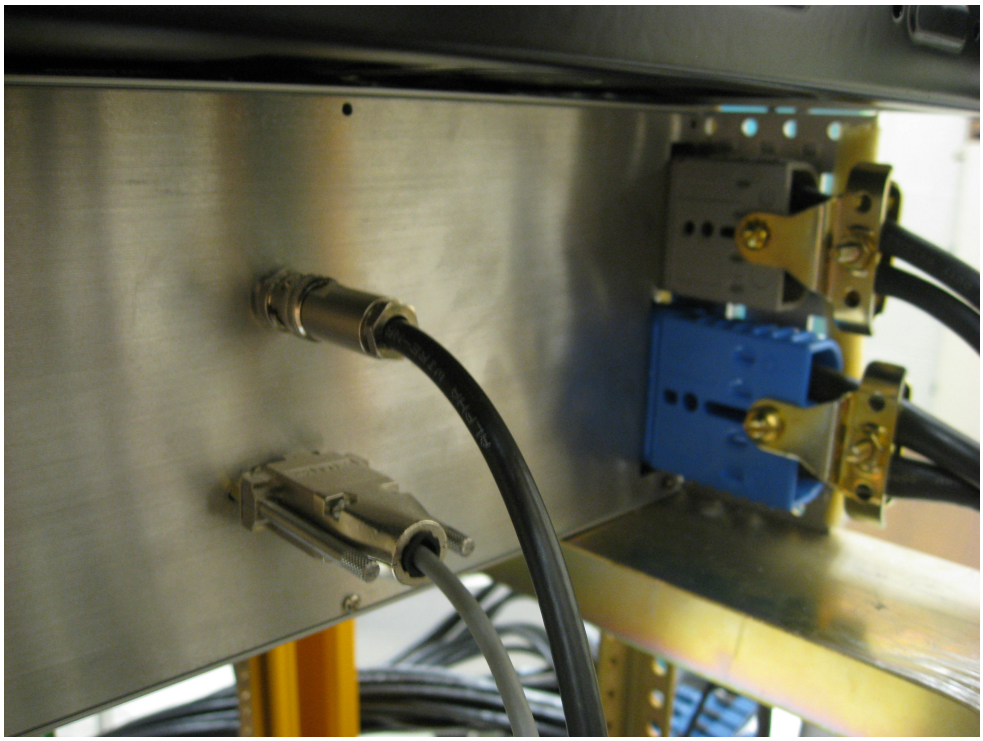


Figure 17. High voltage, sense, 3.3V, and 24V connectors on the back of a PDB.

Figure 18. Rear view of two PDBs in the test rack. There are two ground connections (on left) and one of every other connection.

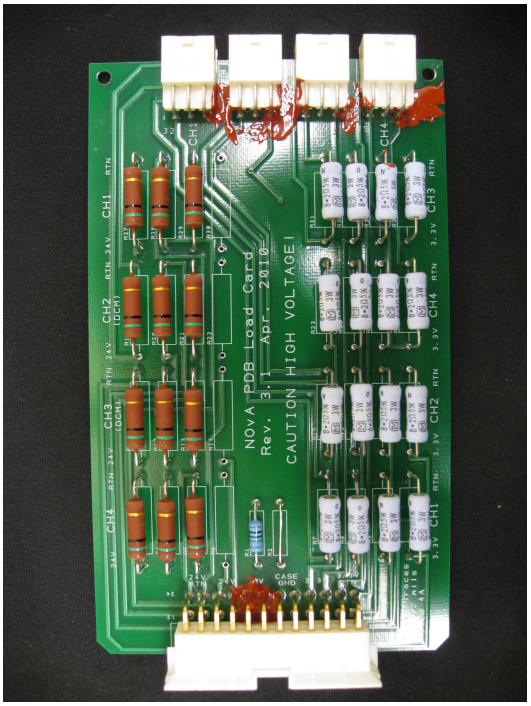


Figure 19. FEB load board used to put the backplane under load when testing the PDBs.

III. Test Procedure

Before running any test make sure that the PDB is properly mounted on the rack with all connectors connected (3.3V, 24V, HV, sense, ground). Connect the lower (prototype) PDB to test the cards and connect the upper PDB to test the PDB components.

Card Testing

1. Connect all cables from the DCM and FEB cards as shown in Figure 7.
2. Turn on the National Instruments PXI crate.
3. Open the LabVIEW project, located at HEP_Private\NOVA\Electrical_Testing\ PDB_automated_testing\LabVIEW\PDB Tests\PDB_Tests.lvproj
4. Open "PDB_Test_Cards_(top).vi".
5. Enable the proper tests and set the start slot, end slot, and number of samples. The default setup has all tests enabled, slots set to 0-16, and the number of samples set to 20. This default setup was used for all card testing during the summer of 2010.
6. Type the indicator card label into the "IND Card Label" control and type the board labels into the "Board Labels" Control. The labels are of the form 3W IND 000XXXX, 3W DCM 000XXXX, 3W FEB 000XXXX.
7. Turn on all power supplies and all e-loads. (see Figure 7)
8. Press the Run arrow in the upper left corner on the Front Panel of PDB_Test_Cards_(top).vi.
9. Enter operator name when prompted.
10. Answer the two popup questions about LEDs.

Backplane Testing

1. Connect all cables from the load boards to the corresponding connectors on the Test Connector Board. The load boards should be installed in the upper PDB. Refer to Figure 9.
2. Turn on the National Instruments PXI crate.

3. Open the LabVIEW project, located at HEP_Private\NOVA\Electrical_Testing\ PDB_automated_testing\LabVIEW\PDB Tests\PDB_Tests.lvproj
4. Open "PDB_Test_Backplane_(top).vi".
5. Set the start slot, end slot, and number of samples. The default setup has slots set to 0-16 and the number of samples set to 20. This default setup was used for all PDB testing during the summer of 2010.
6. Type the backplane label (3W BCK 000XXXX) into the "Backplane Label" control.
7. Plug in the cooling fan.
8. Turn on all power supplies and all e-loads.
9. Press the Run arrow in the upper left corner on the Front Panel of "PDB_Test_Backplane_(top).vi".
10. Enter operator name when prompted.
11. Answer the popup question about LEDs.

Once the Run button has been pressed LabVIEW will open an Excel spreadsheet and begin populating it with data. Upon completion of the test several checks will be performed on the Excel data. When testing the cards, each enabled test (Card, Slot, Current Limit) will have its own Excel spreadsheet. Finally, the operator will be prompted to look over the data. LabVIEW automatically stores each Excel spreadsheet in NOVA\Electrical_Testing \PDB_automated_testing\Test_Data. After reviewing a data file move it from this directory to NOVA\Electrical_Testing\PDB_automated_testing\Test_Data_Reviewed. After moving a file, run variation_correction.vi on this file. See section VII for more information on variation_correction.vi.

IV. LabVIEW Test Programs

The tests are carried out using LabVIEW. All of the testing files are contained in a LabVIEW project (see Section III for the project location). The project ensures that dependencies are saved and loaded correctly. In order to run any program, one should open it from the project browser. There are two main files used for testing: "PDB_Test_Cards_(top).vi" to test cards and "PDB_Test_Backplane_(top).vi" to test all PDB components, specifically

the backplane. "PDB_Test_Cards_(top).vi" is composed of three separate tests: Channel Test, Slot Test, and Current Limit Test. The operator can choose which of these tests to run from the front panel (user interface). "PDB_Test_Backplane_(top).vi" is composed of a single test called Backplane Test.

Channel Test

The Channel Test tests FEB and DCM cards one channel at a time. For each channel, current and voltage measurements are taken at the three power supply outputs and the three electronic loads. The amount of data recorded is determined by the "Num of Samples" control on the Front Panel. The Front Panel is LabVIEW's GUI. With "Num of Samples" set to 20, for example, the Channel Test will take 20 current and voltage measurements of each power supply and each load for every channel. These measurements are taken in steady state (as opposed to ramp up/down). Since each channel is checked individually, this test takes the longest to complete. It takes 25 minutes to run Channel Test on 1 DCM card and 16 FEB cards. Below is pseudocode for Channel Test to give an outline of the actions performed when running the test in LabVIEW.

```
open new excel workbook
write time stamp, labels, and operator name to excel
enable and configure all power supplies
prompt visual test of LEDs and write results to excel
for (slot = startslot; slot <= finalslot; slot ++)
      {
            for (channel = startchannel; channel <= finalchannel; channel ++)
                  {
                        close proper relays
                        enable and configure all e-loads
                        make measurements and write to excel
                        update histograms on front panel
                        disable e-loads
                        open proper relays
                  }
      }
disable power supplies
run data checks on excel data
write time stamp to excel
```

```
save report
```

Slot Test

The Slot Test is just like the Channel Test, except that the cards are tested one full slot (4 channels) at a time, meaning each channel of an FEB card is loaded and current and voltage measurements are taken for the entire card.It takes 6 minutes to run Slot Test on 1 DCM card and 16 FEB cards.

```
open new excel workbook
write time stamp, labels, and operator name to excel
enable and configure all power supplies
prompt visual test of LEDs and write results to excel
for (slot = startslot; slot <= finalslot; slot ++)
      {
            close proper relays
            enable and configure all e-loads
            make measurements and write to excel
            disable e-loads
            open proper relays
      }
disable power supplies
run data checks on excel data
write time stamp to excel
save report
```

Current Limit Test

The Current Limit Test is structured exactly like the Channel Test. In the Current Limit Test however, only the HV e-load is used and data is recorded with the reprogrammable input/output (RIO) card described in Section II. The RIO card is used to digitize analog current and voltage data from the HV power supply at 40K samples/sec. To test the current limiter circuit on the FEB cards, the HV e-load is set to short mode to short the HV supply for a selected channel during data acquisition to check for overcurrent conditions. The relay cables are only rated for 60V, so two 200V zener diodes are used on the Test Connector Board to drop the voltage from 445V to a nominal 45V. Therefore the "short" is not a true short. Figure 20 shows the current limiter test circuit. It takes 6 minutes to run Current Limit Test on 1 DCM card and 16 FEB cards.

```
open new excel workbook
write time stamp, labels, and operator name to excel
enable and configure all power supplies
prompt visual test of LEDs and write results to excel
for (slot = startslot; slot <= finalslot; slot ++)
      {
            for (channel = startchannel; channel <= finalchannel; channel ++)
                  {
                        enable and configure HV e-load
                        begin taking data with FPGA
                        close proper relays to short
                        open proper relays once data has been collected
                        disable e-loads
                  }
      }
disable power supplies
run data checks on excel data
write time stamp to excel
save report
```

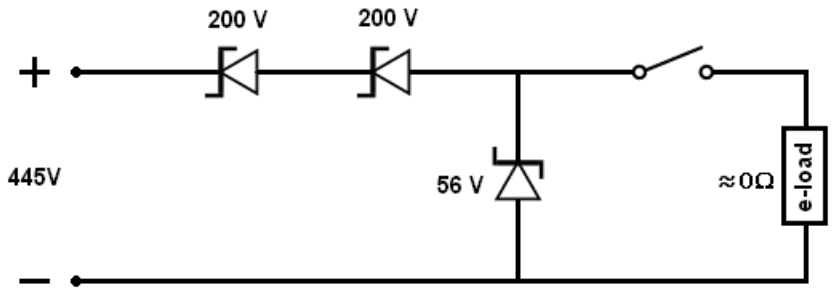


Figure 20. Current limiter test circuit.

Backplane Test

For Backplane Test the two Agilent low voltage supplies are run at maximum current output in constant current mode (100A for the 6V supply and 50A for the 30V supply) and the high voltage supply is run at a nominal 445V. The PDB is put under load with loads boards in place of FEB and DCM cards. Measurements of current and voltage are taken for each channel with the e-loads, just like Channel Test. The e-loads are used for measurement

purposes only, the load is supplied by the load boards. It takes 21 minutes to run Backplane Test.

```
open new excel workbook
write time stamp, labels, and operator name to excel
enable and configure all power supplies
enable loads (used for measurements only)
prompt visual test of LEDs and write results to excel
for (slot = startslot; slot <= finalslot; slot ++)
      {
            for (channel = startchannel; channel <= finalchannel; channel ++)
                  {
                        close proper relays
                        make measurements and write to excel
                        update histograms on front panel
                        open proper relays
                  }
      }
disable power supplies and e-loads
run data checks on excel data
write time stamp to excel
save report
```

For each test the three power supplies are configured to run at 445V, 30V, and 6V. For Channel Test both low voltage loads are configured for constant current mode at 0.985A and for Slot Test they are configured for constant current mode at 4 x 0.985A = 3.94A.

Figure 21 shows part of the Front Panel of PDB Test Cards (top).vi. The three controls at the top (Channel Test Enable, Slot Test Enable, and Current Limit Test Enable) are used to determine which tests will be performed on the cards once testing has begun. The second row of controls (Start Slot, Final Slot, and Num of Samples) determines which cards are tested and how many data samples are recorded for a single measurement. The Indicator card is in the leftmost pair of cardguides or "slot" as it is referred to in this manual. The slot containing the Indicator card is not given a number and is only tested visually. The DCM card is located at slot 0, right next to the Indicator card, and the FEB cards are in slots 1-16 (refer to figure 3). Num of Samples controls the amount of data recorded for Channel Test and Slot Test. Current Limit Test uses an FPGA to record data and is configured separately.

Below these controls are several indicators that display the current state of testing. Pressing the STOP button will end testing as soon as the current slot has finished being tested.

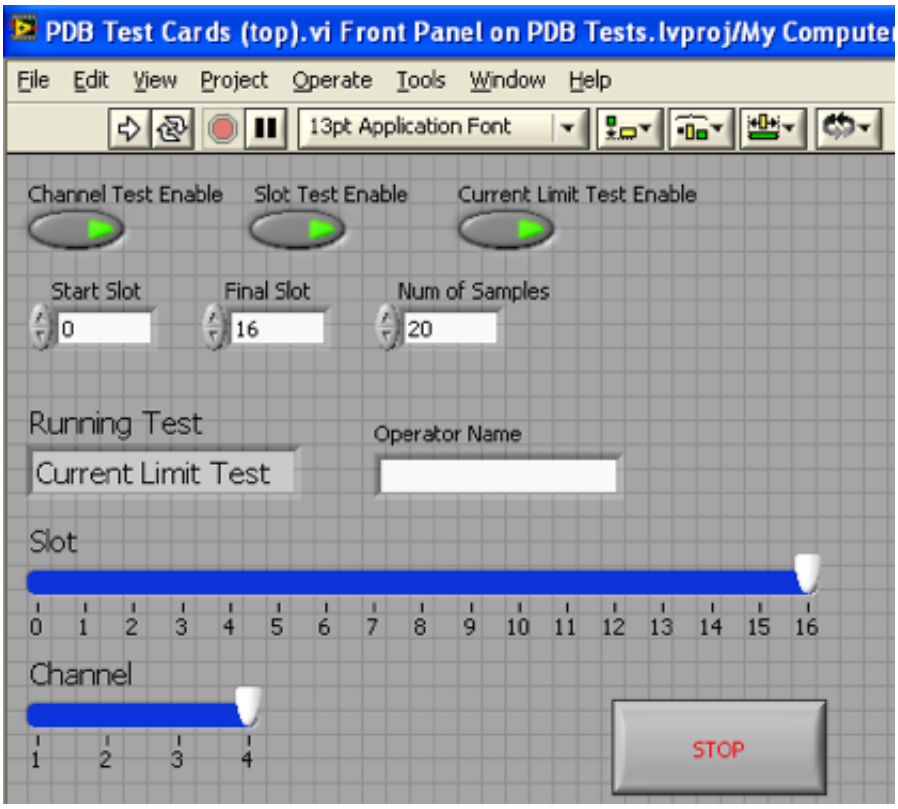


Figure 21. Test configuration and status graphical interface for the cards tests. The Start Slot, Final Slot, and Num of Samples controls apply to each of the three card tests. The green light on a test control indicates that it is enabled and will run once the run arrow is pressed.

Histograms, shown in Figure 22, display data as it is accumulated during Channel Test. These histograms update in real time and are visible on the Front Panel (user interface), just beneath the test configuration controls shown in Figure 21. There is a histogram for the voltage and current of each electronic load. The text box to the left of these histograms displays any measurements that fall outside of their respective histogram bin range and is useful for detecting anomalies in the data. Once a measurement has been flagged as outside the bin range, one should check the excel spreadsheet.

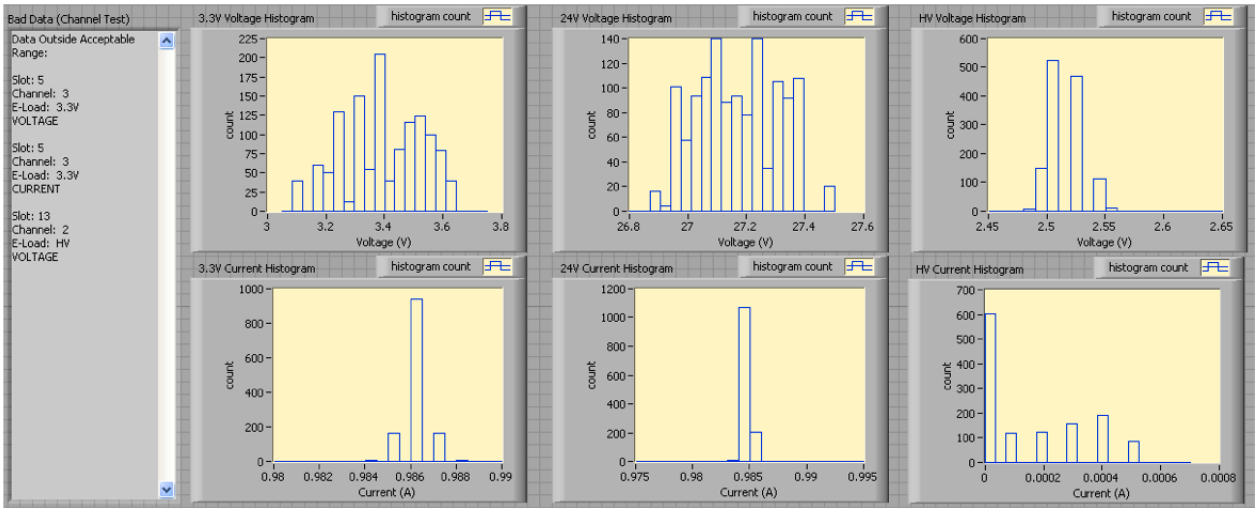


Figure 22. Histograms on front panel.

V. Data Analysis

During testing, LabVIEW generates an Excel file containing the test data. After collecting the data for a particular test, the LabVIEW test program analyzes the data in the Excel file using LabVIEW's Excel tools. For the Channel, Slot, and Backplane tests the averages and standard deviations of the measurements for each instrument are computed. These statistics are then used to check each data point for that test run. If a data point is not within 3 standard deviations of the average for that test run, then the Excel cell containing that data point is highlighted. Each data point is also compared to an accepted value. If a data point is not within a certain range of this accepted value its cell is highlighted. The ranges of accepted values have been established through much testing. Figures 31, 32, and 33 show the acceptance ranges for the Channel, Slot, and Backplane Tests. By comparing test data to set accepted values any problems with the cards or backplanes will be found.

Figure 23 shows how the data looks in excel. There is a sheet containing all of the data, a sheet containing the analysis information, and (for the Channel Test) a sheet containing the LabVIEW histograms. Figure 24 shows how data is highlighted if it is outside the acceptance range. The color of the highlighting corresponds to the criteria that the data failed to meet. Figure 25 shows the analysis tab, where four acceptance ranges are listed. The top two are for checking the FEB card data (one using the statistics of that test and one using a predetermined acceptance range). The bottom two ranges are used to check the DCM card data. The row labeled "DCM Diff" shows the offset of the expected values of measurements on the DCM card vs measurements on FEB cards.

	A	B	C	D	E	F	G	H	I
1	**Channel Test**		**Start**	**7/12/10**	**4:19 PM**		**End**	**7/12/10**	**4:43 PM**
2	OPR: S. Goadhouse								
3									
4	3W IND 0000002	LED PASS	Other LEDs:	LED PASS					
5									
6	*Initial Measurements:*				*5.9999*	*0.87*	*30*	*0.453*	*445*
7									
8	**Board Label**	**Slot**	**Channel**	**Sample**	**PS6V V**	**PS6V I**	**PS30V V**	**PS30V I**	**PSHV V**	**PSHV**
9	3W DCM 0000002	slot DCM	channel 1	1	6.0001	0.87	30	1.435	445	
10	3W DCM 0000002	slot DCM	channel 1	2	6.0001	0.87	30.001	1.435	441	
11	3W DCM 0000002	slot DCM	channel 1	3	6.0001	0.87	30.001	1.435	445	
12	3W DCM 0000002	slot DCM	channel 1	4	6.0001	0.87	30.001	1.435	446	
13	3W DCM 0000002	slot DCM	channel 1	5	6.0001	0.87	30	1.435	446	
14	3W DCM 0000002	slot DCM	channel 1	6	6.0001	0.87	30.001	1.435	446	
15	3W DCM 0000002	slot DCM	channel 1	7	6.0001	0.87	30.001	1.435	448	
16	3W DCM 0000002	slot DCM	channel 1	8	6.0001	0.87	30	1.435	446	
17	3W DCM 0000002	slot DCM	channel 1	9	6.0001	0.87	30	1.435	447	
18	3W DCM 0000002	slot DCM	channel 1	10	6.0001	0.87	30	1.435	446	
19	3W DCM 0000002	slot DCM	channel 1	11	6.0001	0.87	30	1.435	442	
20	3W DCM 0000002	slot DCM	channel 1	12	6.0001	0.87	30	1.435	447	
21	3W DCM 0000002	slot DCM	channel 1	13	6.0001	0.87	30	1.435	445	
22	3W DCM 0000002	slot DCM	channel 1	14	6.0001	0.87	30.001	1.436	445	
23	3W DCM 0000002	slot DCM	channel 1	15	6.0002	0.87	30	1.436	444	
24	3W DCM 0000002	slot DCM	channel 1	16	6.0001	0.87	30	1.435	446	
25	3W DCM 0000002	slot DCM	channel 1	17	6.0001	0.87	30	1.435	447	
26	3W DCM 0000002	slot DCM	channel 1	18	6.0001	0.87	30	1.435	441	
27	3W DCM 0000002	slot DCM	channel 1	19	6.0001	0.87	30	1.435	447	
28	3W DCM 0000002	slot DCM	channel 1	20	6.0001	0.87	30.001	1.436	446	
29	3W DCM 0000002	slot DCM	channel 2	1	6.0001	0.87	30	1.435	448	
30	3W DCM 0000002	slot DCM	channel 2	2	6.0001	0.87	30.001	1.436	444	
31	3W DCM 0000002	slot DCM	channel 2	3	6.0001	0.87	30.001	1.435	445	
32	3W DCM 0000002	slot DCM	channel 2	4	6.0001	0.87	30.001	1.435	446	
33	3W DCM 0000002	slot DCM	channel 2	5	6.0001	0.87	30.001	1.435	444	
34	3W DCM 0000002	slot DCM	channel 2	6	6.0001	0.87	30.001	1.436	446	
35	3W DCM 0000002	slot DCM	channel 2	7	6.0001	0.87	30	1.436	447	
36	3W DCM 0000002	slot DCM	channel 2	8	6.0001	0.87	30.001	1.436	443	

Figure 23. Excel spreadsheet: Data worksheet for the Channel Test.

	A	B	C	D	E	F	G	H	I
341	3W FEB 0000020	slot 4	channel 1	13	6.0001	1.85	30.001	1.436	446
342	3W FEB 0000020	slot 4	channel 1	14	6.0001	1.85	30.001	1.436	446
343	3W FEB 0000020	slot 4	channel 1	15	6.0001	1.85	30.001	1.436	440
344	3W FEB 0000020	slot 4	channel 1	16	6.0002	1.85	30.001	1.436	445
345	3W FEB 0000020	slot 4	channel 1	17	6.0001	1.86	30.001	1.436	449
346	3W FEB 0000020	slot 4	channel 1	18	6.0001	1.85	30.001	1.436	447
347	3W FEB 0000020	slot 4	channel 1	19	6.0001	1.85	30.001	1.436	445
348	3W FEB 0000020	slot 4	channel 1	20	6.0001	1.85	30.001	1.436	446
349	3W FEB 0000020	slot 4	channel 2	1	6.0001	0.87	30.001	0.454	447
350	3W FEB 0000020	slot 4	channel 2	2	6.0001	0.87	30.001	0.454	445
351	3W FEB 0000020	slot 4	channel 2	3	6.0001	0.87	30	0.454	446
352	3W FEB 0000020	slot 4	channel 2	4	6.0001	0.87	30.001	0.454	445
353	3W FEB 0000020	slot 4	channel 2	5	6.0001	0.87	30.001	0.454	444
354	3W FEB 0000020	slot 4	channel 2	6	6.0001	0.87	30.001	0.454	445
355	3W FEB 0000020	slot 4	channel 2	7	6.0002	0.87	30.001	0.454	446
356	3W FEB 0000020	slot 4	channel 2	8	6.0001	0.87	30.001	0.454	441
357	3W FEB 0000020	slot 4	channel 2	9	6.0001	0.87	30.001	0.454	445
358	3W FEB 0000020	slot 4	channel 2	10	6.0001	0.87	30.001	0.454	447
359	3W FEB 0000020	slot 4	channel 2	11	6.0001	0.87	30.001	0.454	446
360	3W FEB 0000020	slot 4	channel 2	12	6.0001	0.87	30.001	0.454	445
361	3W FEB 0000020	slot 4	channel 2	13	6.0001	0.87	30.001	0.454	447
362	3W FEB 0000020	slot 4	channel 2	14	6.0001	0.87	30.001	0.454	446
363	3W FEB 0000020	slot 4	channel 2	15	6.0001	0.87	30.001	0.454	447
364	3W FEB 0000020	slot 4	channel 2	16	6.0001	0.87	30.001	0.454	446
365	3W FEB 0000020	slot 4	channel 2	17	6.0001	0.87	30.001	0.454	446
366	3W FEB 0000020	slot 4	channel 2	18	6.0001	0.87	30	0.454	450
367	3W FEB 0000020	slot 4	channel 2	19	6.0001	0.87	30.001	0.454	446
368	3W FEB 0000020	slot 4	channel 2	20	6.0001	0.87	30.001	0.454	447
369	3W FEB 0000020	slot 4	channel 3	1	6.0001	1.86	30.001	1.436	447
370	3W FEB 0000020	slot 4	channel 3	2	6.0002	1.85	30.001	1.436	446
371	3W FEB 0000020	slot 4	channel 3	3	6.0002	1.86	30.001	1.436	445
372	3W FEB 0000020	slot 4	channel 3	4	6.0001	1.86	30.001	1.436	441
373	3W FEB 0000020	slot 4	channel 3	5	6.0002	1.85	30.001	1.436	443
374	3W FEB 0000020	slot 4	channel 3	6	6.0001	1.85	30.001	1.436	447
375	3W FEB 0000020	slot 4	channel 3	7	6.0001	1.85	30.001	1.436	446
376	3W FEB 0000020	slot 4	channel 3	8	6.0001	1.85	30.001	1.436	445
377	3W FEB 0000020	slot 4	channel 3	9	6.0001	1.85	30.001	1.436	446

Figure 24. Excel spreadsheet: Data worksheet showing highlighted cells which indicate data outside acceptance ranges.

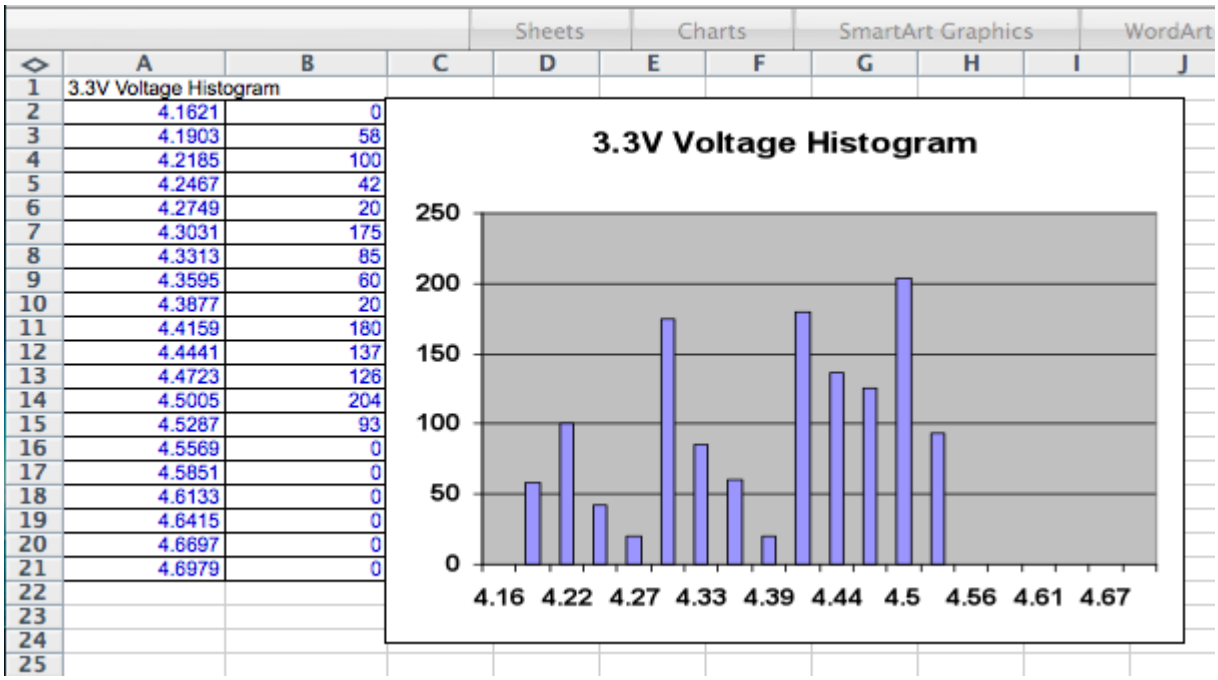
	A	B	C	D	E	F	G	H	I	J
1										
2										
3										
4										
5			PS6V V	PS6V I	PS30V V	PS30V I	PSHV V	PSHV I	LD3V3 V	LD3V3 I
6		Calc Avg	6.00016	1.83595	30.00078	1.42081	445.41364	0.00123	4.32254	0.97101
7		Calc Std Dev	0.00005	0.11989	0.00041	0.11996	1.72309	0.00002	0.54528	0.12048
8		Norm Avg	6.0002	1.84	30.001	1.421	445	0.00123	4.323	0.971
9		Norm Range	0.0002	0.36	0.002	0.36	7	6.00E-05	1.636	0.362
10		*Upper Bound*	*6.0004*	*2.2*	*30.003*	*1.781*	*452*	*0.00129*	*5.959*	*1.333*
11		*Lower Bound*	*6*	*1.48*	*29.999*	*1.061*	*438*	*0.00117*	*2.687*	*0.609*
12										
13										
14		Master Avg	6.00015	1.85	30	1.435	445	0.00122	4.43	0.985
15		Master Range	0.0003	0.02	0.005	0.003	9	5.00E-05	0.282	0.005
16		*Upper Bound*	*6.00045*	*1.87*	*30.005*	*1.438*	*454*	*0.00127*	*4.712*	*0.99*
17		*Lower Bound*	*5.99985*	*1.83*	*29.995*	*1.432*	*436*	*0.00117*	*4.148*	*0.98*
18										
19										
20		DCM Diff	0	0	0	0	0	0	0	0
21		Norm DCM Avg	6.0002	1.84	30.001	1.421	445	0.00123	4.323	0.971
22		Norm DCM Range	0.0002	0.36	0.002	0.36	7	6.00E-05	1.636	0.362
23		*Upper Bound*	*6.0004*	*2.2*	*30.003*	*1.781*	*452*	*0.00129*	*5.959*	*1.333*
24		*Lower Bound*	*6*	*1.48*	*29.999*	*1.061*	*438*	*0.00117*	*2.687*	*0.609*
25										
26										
27		Master DCM Avg	6.00015	1.85	30	1.435	445	0.00122	4.43	0.985
28		Master DCM Range	0.0003	0.02	0.005	0.003	9	5.00E-05	0.282	0.005
29		*Upper Bound*	*6.00045*	*1.87*	*30.005*	*1.438*	*454*	*0.00127*	*4.712*	*0.99*
30		*Lower Bound*	*5.99985*	*1.83*	*29.995*	*1.432*	*436*	*0.00117*	*4.148*	*0.98*
31										
32										
33										
34										
35										
36										
37										

Figure 25. Excel spreadsheet: Analysis worksheet showing acceptance ranges and their color coding.

	I	J	K	L	M	N	O	P	Q	R	S	T
5	LD3V3 V	LD3V3 I	LD24V V	LD24V I	LDHV V	LDHV I						
6	4.32254	0.97101	27.73738	0.96906	2.46457	0.00014						
7	0.54528	0.12048	3.44363	0.12024	0.30574	0.00016		F349		F349		
8	4.323	0.971	27.74	0.969	2.46	0.0001		F350		F350		
9	1.636	0.362	10.34	0.361	0.92	0.0005		F351		F351		
10	5.959	1.333	38.08	1.33	3.38	0.0006		F352		F352		
11	2.687	0.609	17.4	0.608	1.54	-0.0004		F353		F353		
12								F354		F354		
13								F355		F355		
14	4.43	0.985	28.2	0.9825	2.5	0.0003		F356		F356		
15	0.282	0.005	0.32	0.021	0.05	0.0003		F357		F357		
16	4.712	0.99	28.52	1.0035	2.55	0.0006		F358		F358		
17	4.148	0.98	27.88	0.9615	2.45	0		F359		F359		
18								F360		F360		
19								F361		F361		
20	0	0	0.1	0	0	0		F362		F362		
21	4.323	0.971	27.84	0.969	2.46	0.0001		F363		F363		
22	1.636	0.362	10.34	0.361	0.92	0.0005		F364		F364		
23	5.959	1.333	38.18	1.33	3.38	0.0006		F365		F365		
24	2.687	0.609	17.5	0.608	1.54	-0.0004		F366		F366		
25								F367		F367		
26								F368		F368		
27	4.43	0.985	28.3	0.9825	2.5	0.0003		H349		H349		
28	0.282	0.005	0.32	0.021	0.05	0.0003		H350		H350		
29	4.712	0.99	28.62	1.0035	2.55	0.0006		H351		H351		
30	4.148	0.98	27.98	0.9615	2.45	0		H352		H352		
31								H353		H353		
32								H354		H354		
33								H355		H355		
34								H356		H356		
35								H357		H357		
36								H358		H358		
37								H359		H359		
38								H360		H360		

Figure 26. Excel spreadsheet: Analysis worksheet showing the list of cells on the right containing data that failed each test.

Figure 26 shows the rest of the analysis sheet, where the cells containing bad data are listed. Figure 27 shows the third sheet containing the LabVIEW histograms. This sheet is only present for the Channel test data.



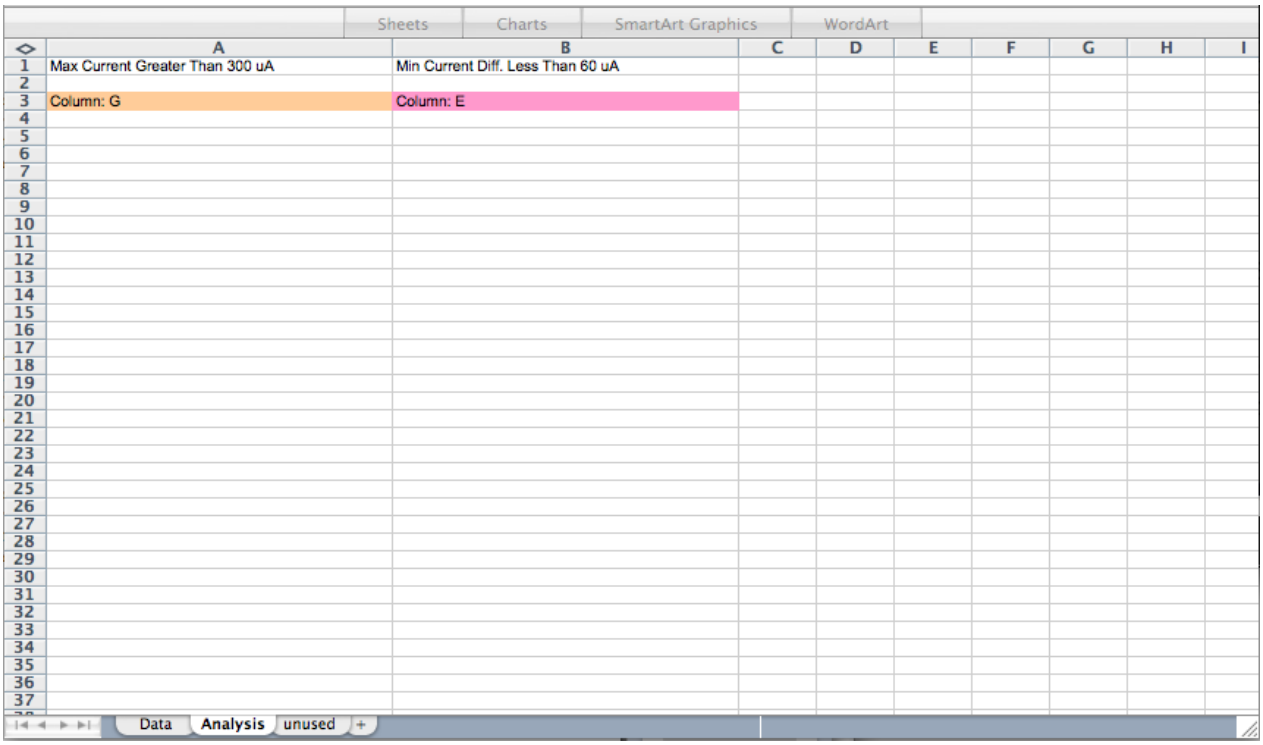
	A	B
1	3.3V Voltage Histogram	
2	4.1621	0
3	4.1903	58
4	4.2185	100
5	4.2467	42
6	4.2749	20
7	4.3031	175
8	4.3313	85
9	4.3595	60
10	4.3877	20
11	4.4159	180
12	4.4441	137
13	4.4723	126
14	4.5005	204
15	4.5287	93
16	4.5569	0
17	4.5851	0
18	4.6133	0
19	4.6415	0
20	4.6697	0
21	4.6979	0

Figure 27. Excel spreadsheet: Histograms worksheet for Channel Test data.

Figure 28 is an example of an Excel spreadsheet for the Current Limit Test. Two methods are used to check the Current Limit data. The first is to simply highlight any cell that corresponds to a HV current $> 300\mu$A. A current larger than 300μA indicates that the current is not being limited properly. As a second check, the difference in the minimum closed current (current while shorted) and the maximum open current (current before short) is computed. If this difference is less than 60μA, the cell is highlighted. A value $< 60\mu$A means that the current limiter circuit is not being engaged, which indicates a problem. Figure 29 shows the analysis sheet where any highlighted cells are listed. Figure 30 shows a graph of the typical response to shorting.

	A	B	C	D	E	F	G	H	I
1	**Current Limit Test**		**Start**	**7/16/10**	**11:43 AM**		**End**	**7/16/10**	**11:44 AM**
2	OPR: S. Goadhouse								
3									
4									
5	**Board Label**	V DCM 0000007	V DCM 0000007	V DCM 0000007	V DCM 0000007	V FEB 0000097	V FEB 0000097	V FEB 0000097	V FEB 0000097
6	**Slot**	slot DCM	slot DCM	slot DCM	slot DCM	slot 1	slot 1	slot 1	slot 1
7	**Channel**	channel 3	channel 3	channel 4	channel 4	channel 1	channel 1	channel 2	channel 2
8	**Metric**	HV Voltage	HV Current	HV Voltage	HV Current	HV Voltage	HV Current	HV Voltage	HV Current
9	**Min**	437	48	439	41	436	43	438	17
10	**Max**	450	205	450	74	450	1379	450	190
11	**Diff in Max/Min**	13	157	11	33	14	1336	12	173
12	**Max Open Current**		76.00		74.00		73.00		43.00
13	**Min Shorted Current**		173.00		47.00		1328.00		159.00
14	**Min Current Diff**		97.00		-27.00		1255.00		116.00
15	**Data**	444	62	446	69	448	66	446	32
16		444	64	446	67	444	62	444	28
17		447	66	448	68	446	62	445	32
18		444	68	443	63	447	63	446	31
19		445	67	447	67	445	62	445	35
20		446	67	447	68	447	65	445	32
21		443	63	445	68	446	61	446	31
22		446	66	447	66	443	58	445	34
23		446	67	445	63	447	63	444	28
24		444	66	444	61	445	62	446	32
25		447	68	447	65	444	58	443	29
26		445	67	444	60	447	63	446	34
27		445	67	446	65	440	48	445	34
28		447	67	446	60	446	64	443	27
29		445	69	446	70	446	60	446	33
30		445	68	446	65	443	60	444	31
31		447	68	448	66	446	63	445	32
32		444	65	445	67	446	60	447	33
33		445	65	446	62	444	62	444	31
34		446	67	447	66	447	64	445	31

Figure 28. Excel spreadsheet: Data worksheet for the Current Limit Test. The columns contain HV voltage and current data for the different channels of the DCM and FEB cards.



	A	B	C	D	E	F	G	H	I
1	Max Current Greater Than 300 uA	Min Current Diff. Less Than 60 uA							
2									
3	Column: G	Column: E							

Sheets Charts SmartArt Graphics WordArt

Data Analysis unused +

Figure 29. Excel spreadsheet: Analysis worksheet for the Current Limit Test showing the list of data outside acceptance ranges.

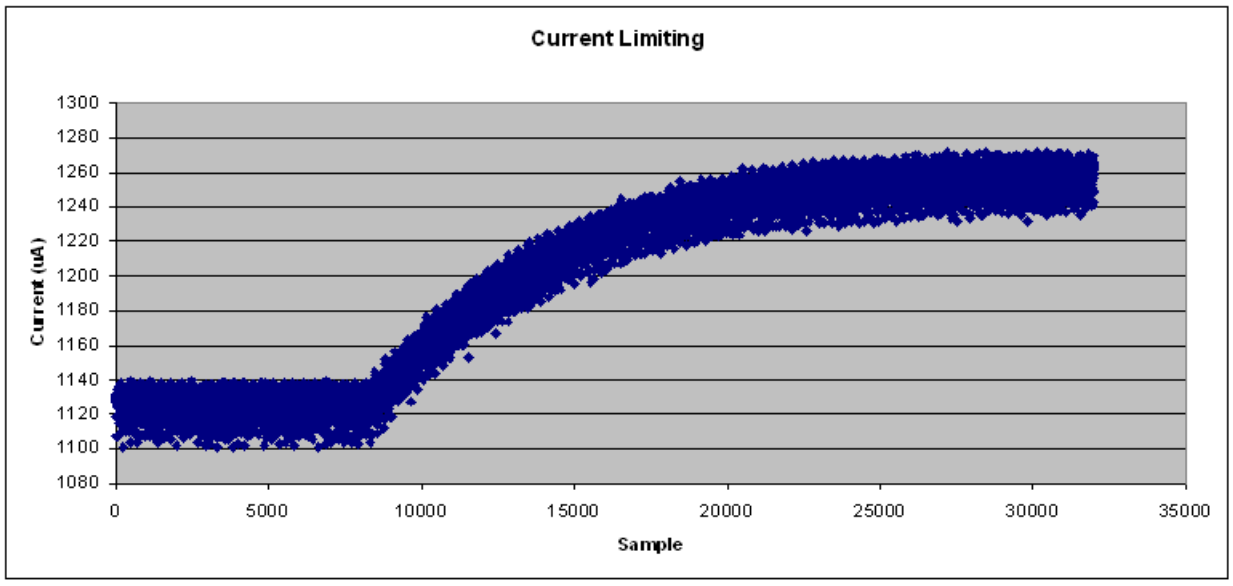


Figure 30. Graph of Current Limit data showing the response during a short. This is not automatically produced during testing.

	PS6V V	PS6V I	PS30V V	PS30V I	PSHV V	PSHV I
Master FEB Avg	6.00015	1.85	30	1.435	445	0.00125
Master FEB Range	0.001	0.02	0.005	0.003	11	0.00011
Upper Bound	*6.00115*	*1.87*	*30.005*	*1.438*	*456*	*0.00136*
Lower Bound	*5.99915*	*1.83*	*29.995*	*1.432*	*434*	*0.00114*
Master DCM Avg	6.00015	1.85	30	1.435	445	0.00125
Master DCM Range	0.001	0.02	0.005	0.003	11	0.00011
Upper Bound	*6.00115*	*1.87*	*30.005*	*1.438*	*456*	*0.00136*
Lower Bound	*5.99915*	*1.83*	*29.995*	*1.432*	*434*	*0.00114*

	LD3V3 V	LD3V3 I	LD24V V	LD24V I	LDHV V	LDHV I
Master FEB Avg	4.43	0.985	28.2	0.9825	2.5	0.0003
Master FEB Range	0.282	0.005	0.32	0.021	0.08	0.0003
Upper Bound	*4.712*	*0.99*	*28.52*	*1.0035*	*2.58*	*0.0006*
Lower Bound	*4.148*	*0.98*	*27.88*	*0.9615*	*2.42*	*0*
Master DCM Avg	4.43	0.985	28.3	0.9825	2.5	0.0003
Master DCM Range	0.282	0.005	0.32	0.021	0.08	0.0003
Upper Bound	*4.712*	*0.99*	*28.62*	*1.0035*	*2.58*	*0.0006*
Lower Bound	*4.148*	*0.98*	*27.98*	*0.9615*	*2.42*	*0*

Figure 31. Ranges of accepted values for the Channel Test.

	PS6V V	PS6V I	PS30V V	PS30V I	PSHV V	PSHV I
Master FEB Avg	6.00015	4.79	30	4.385	445	0.00144
Master FEB Range	0.001	0.02	0.005	0.003	11	0.00015
Upper Bound	*6.00115*	*4.81*	*30.005*	*4.388*	*456*	*0.00159*
Lower Bound	*5.99915*	*4.77*	*29.995*	*4.382*	*434*	*0.00129*
Master DCM Avg	6.00015	2.83	30	4.385	445	0.00131
Master DCM Range	0.001	0.02	0.005	0.003	11	0.00015
Upper Bound	*6.00115*	*2.85*	*30.005*	*4.388*	*456*	*0.00146*
Lower Bound	*5.99915*	*2.81*	*29.995*	*4.382*	*434*	*0.00116*

	LD3V3 V	LD3V3 I	LD24V V	LD24V I	LDHV V	LDHV I
Master FEB Avg	4.29	3.94	28	3.935	2.5	0.0005
Master FEB Range	0.21	0.005	0.214	0.005	0.3	0.0005
Upper Bound	*4.5*	*3.945*	*28.214*	*3.94*	*2.8*	*0.001*
Lower Bound	*4.08*	*3.935*	*27.786*	*3.93*	*2.2*	*0*
Master DCM Avg	4.39	1.97	28.3	3.935	2.5	0.0004
Master DCM Range	0.21	0.005	0.214	0.005	0.3	0.0005
Upper Bound	*4.6*	*1.975*	*28.514*	*3.94*	*2.8*	*0.0009*
Lower Bound	*4.18*	*1.965*	*28.086*	*3.93*	*2.2*	*-0.0001*

Figure 32. Ranges of accepted values for the Slot Test.

	PS6V V	PS6V I	PS30V V	PS30V I	PSHV V	PSHV I
Master FEB Avg	3.314	100.03	3.51	50	445	0.00228
Master FEB Range	0.012	0.02	0.012	0.003	15	0.000212
Upper Bound	*3.326*	*100.05*	*3.522*	*50.003*	*460*	*0.002492*
Lower Bound	*3.302*	*100.01*	*3.498*	*49.997*	*430*	*0.002068*
Master DCM Avg	3.314	100.03	3.51	50	445	0.00228
Master DCM Range	0.012	0.02	0.021	0.003	15	0.000212
Upper Bound	*3.326*	*100.05*	*3.531*	*50.003*	*460*	*0.002492*
Lower Bound	*3.302*	*100.01*	*3.489*	*49.997*	*430*	*0.002068*

	LD3V3 V	LD3V3 I	LD24V V	LD24V I	LDHV V	LDHV I
Master FEB Avg	3.093	1.454	3.36	0.663	445.85	4.45E-05
Master FEB Range	0.035	0.019	0.09	0.016	16.35	3.30E-06
Upper Bound	*3.128*	*1.473*	*3.45*	*0.679*	*462.2*	*4.78E-05*
Lower Bound	*3.058*	*1.435*	*3.27*	*0.647*	*429.5*	*4.12E-05*
Master DCM Avg	3.093	1.454	3.36	2.42	445.85	4.45E-05
Master DCM Range	0.035	0.019	0.2	0.106	16.35	3.30E-06
Upper Bound	*3.128*	*1.473*	*3.56*	*2.526*	*462.2*	*4.78E-05*
Lower Bound	*3.058*	*1.435*	*3.16*	*2.314*	*429.5*	*4.12E-05*

Figure 33. Ranges of accepted values for the Backplane Test.

VII. Calibration of Testing System

In the testing system there is an inherent variation in the impedance of each channel. This variation is due to the different lengths of the traces on the Test Connector Boards, as well as differences in the impedances of the relay modules. This variation spreads the FEB voltages out over a range of more than 300mV under our test conditions. To remedy this, a set of calibration measurements was performed. FEB 0001 was plugged into slot 1 of the prototype PBD, with all other slots empty. Channel 1 of this FEB card was successively plugged into each of the 64 channels on the Test Connector Boards and measurements were recorded for each of the three voltages on each channel. These measurement were taken using the Channel Test in "PDB_Test_Cards_(top).vi". The maximum value for each of the three voltages (FEB, TEC, APD) was then identified. A correction factor was calculated for the FEB and TEC voltages of each channel such that upon multiplying by the correction factor, each channel would read the maximum value for each voltage. Since the APD operates on very small currents, any difference in the APD voltages is negligible and needs no correction.

A LabVIEW program was created to apply these corrections to Excel spreadsheets containing data for Channel Tests. The program is located in the LabVIEW Project file: NOVA\Electrical_Testing\PDB_automated_testing\LabVIEW\PDB Tests\PDB_Tests.lvproj under the name variation_correction.vi. This program corrects the FEB and TEC voltage measurements taken by the electronic loads for slots 1-16. Figures 34 and 35 show the effect of the corrections on both low voltage measurements.

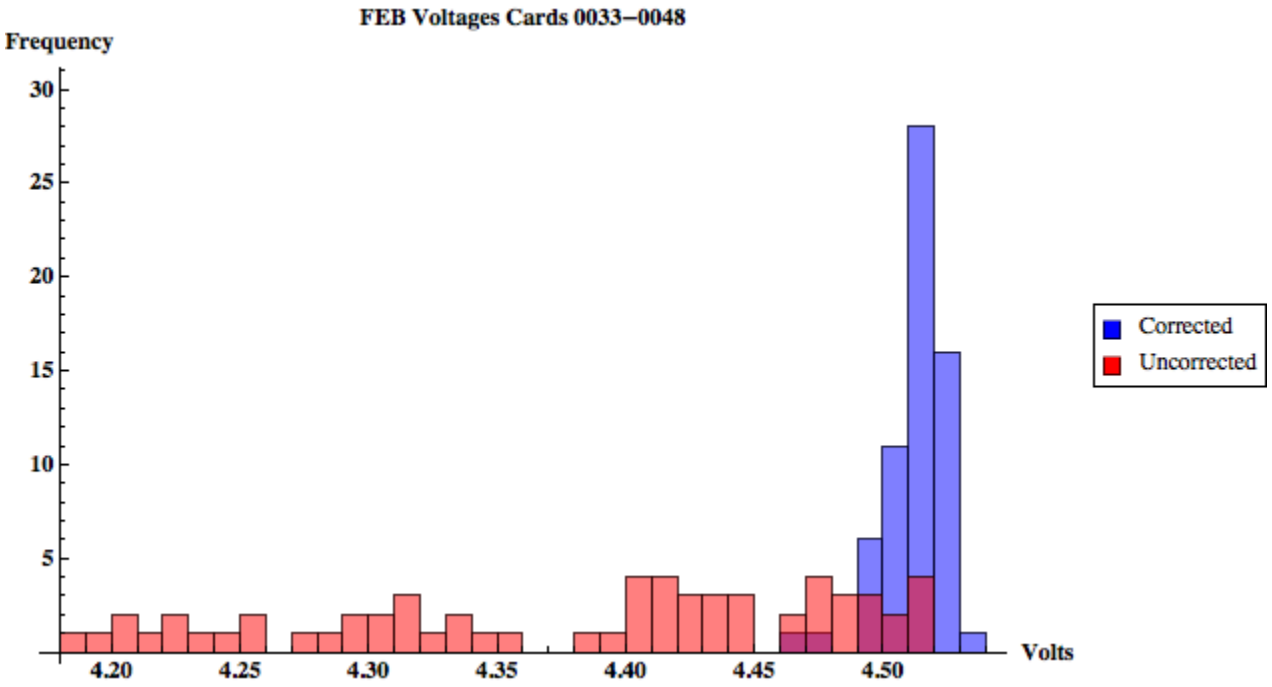


Figure 34. Variation in average FEB voltage on each channel.

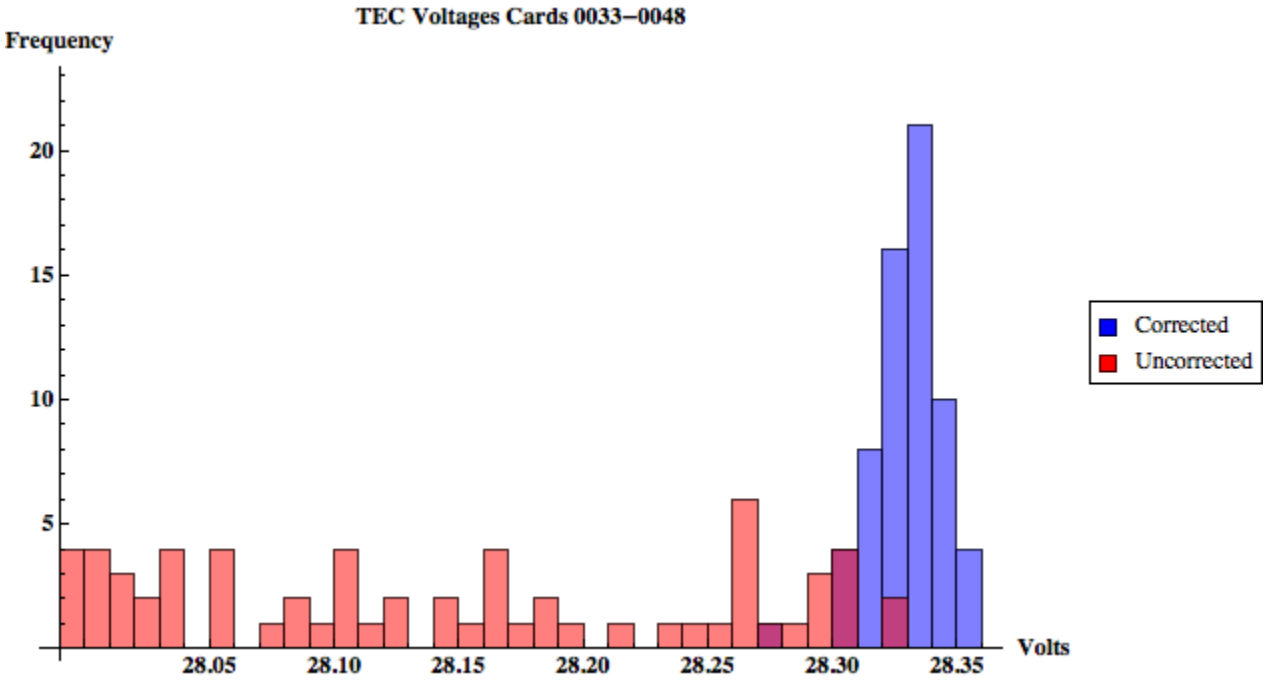


Figure 35. Variation in average TEC voltage on each channel.

	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8
Channel 1 3.3	1.014	1.041	1.045	1.075	1.018	1.047	1.045	1.075
Channel 1 24	1.003	1.005	1.010	1.005	1.003	1.006	1.010	1.005
Channel 1 HV	1.002	1.001	1.002	1.002	1.003	1.003	1.005	1.004
Channel 2 3.3	1.016	1.064	1.023	1.062	1.019	1.070	1.027	1.063
Channel 2 24	1.006	1.008	1.011	1.011	1.007	1.008	1.012	1.011
Channel 2 HV	1.004	1.002	1.001	1.000	1.003	1.005	1.004	1.004
Channel 3 3.3	1.000	1.010	1.009	1.023	1.002	1.012	1.009	1.023
Channel 3 24	1.008	1.001	1.011	1.002	1.008	1.001	1.011	1.002
Channel 3 HV	1.001	1.000	1.001	1.004	1.003	1.003	1.004	1.002
Channel 4 3.3	1.001	1.046	1.004	1.039	1.004	1.048	1.005	1.040
Channel 4 24	1.009	1.001	1.011	1.000	1.009	1.002	1.011	1.000
Channel 4 HV	1.000	1.003	1.002	1.004	1.006	1.002	1.004	1.005

	Slot 9	Slot 10	Slot 11	Slot12	Slot 13	Slot 14	Slot 15	Slot 16
Channel 1 3.3	1.020	1.050	1.048	1.074	1.019	1.044	1.047	1.075
Channel 1 24	1.003	1.006	1.010	1.006	1.002	1.006	1.010	1.005
Channel 1 HV	1.006	1.005	1.008	1.006	1.004	1.002	1.009	1.006
Channel 2 3.3	1.023	1.071	1.028	1.064	1.020	1.068	1.025	1.062
Channel 2 24	1.007	1.008	1.012	1.011	1.006	1.008	1.012	1.012
Channel 2 HV	1.005	1.006	1.009	1.006	1.006	1.008	1.007	1.007
Channel 3 3.3	1.007	1.014	1.012	1.026	1.003	1.013	1.009	1.023
Channel 3 24	1.008	1.002	1.011	1.002	1.008	1.001	1.011	1.002
Channel 3 HV	1.005	1.004	1.006	1.006	1.004	1.006	1.006	1.008
Channel 4 3.3	1.009	1.050	1.007	1.043	1.006	1.051	1.005	1.038
Channel 4 24	1.009	1.002	1.011	1.001	1.009	1.002	1.011	1.000
Channel 4 HV	1.006	1.006	1.006	1.005	1.006	1.008	1.007	1.006

Figure 36. Multiplicative correction factors for each voltage on each channel. The program variation_correction.vi uses these values to correct the Excel spreadsheets.

VI. Tips and Tricks

- Don't just hit the Run button and walk away. Make sure to answer the popup questions at the beginning of the test or it won't start.
- One may use the scroll bars to move around the Excel spreadsheet during testing but don't click on any cells, as this may cause an error in LabVIEW.
- If you are receiving communication errors during testing, try unplugging the USB hub from the PXI crate and plugging it back in. Note: this has caused windows to reboot in the past, so make sure nothing would be lost in the event of a reboot. You can also try restarting the device giving the communication error.
- In order to seat the relay cables properly into the relay modules, it may be necessary to wiggle them up and down while tightening.
- Don't use the red "abort" button in the LabVIEW toolbar to stop a test. Use the STOP button on the front panel and wait for the program to stop. When the abort button is used the communication to the power supplies or e-loads is not closed properly, which causes problems when starting the test again.

References

[1] Spellman Corporate Headquarters. 475 Wireless Blvd. Hauppauge, New York 11788.

[2] Agilent Technologies Headquarters. 5301 Stevens Creek Blvd. Santa Clara, CA 95051.

[3] Tyco Electronics Corporation. 1050 Westlakes Drive. Berwyn, PA 19312.